Claims

What is claimed is:

1. A method for detecting degradation in an integrated circuit comprising the steps of:

providing a monitor built-in self-test (MBIST) engine;

providing at least one monitor element coupled to said MBIST engine; said at least one monitor element being defined by predefined circuit elements in the integrated circuit;

utilizing said MBIST engine for controlling operation of said at least one monitor element and communicating monitor bits; and

identifying degradation of signal, timing and voltage margins utilizing said at least one monitor element.

2. A method for detecting degradation in an integrated circuit as recited in claim 1 wherein the step of providing at least one monitor element coupled to said MBIST engine includes the steps of providing at least one monitor element defined by unused circuit elements or instantiations of said unused circuit elements in the integrated circuit.

3. A method for detecting degradation in an integrated circuit as recited in claim 1 wherein the step of providing a monitor built-in self-test (MBIST) engine includes providing MBIST control circuitry and MBIST registers.

4. A method for detecting degradation in an integrated circuit as recited in claim 1 wherein the step of providing at least one monitor element coupled to said MBIST engine includes the steps of providing at least one monitor element used as a monitor bit line.

5. A method for detecting degradation in an integrated circuit as recited in claim 1 wherein the step of providing at least one monitor element coupled to said MBIST engine includes the steps of providing at least one monitor element used as a monitor word line.

6. A method for detecting degradation in an integrated circuit as recited in claim 1 wherein the step of providing at least one monitor element coupled to said MBIST engine includes the steps of providing at least one monitor element defined by a separate monitor array; said separate monitor array including unique word lines, bit lines, and control and sense circuitry.

7. A method for detecting degradation in an integrated circuit as recited in claim 1 wherein said separate monitor array is placed proximate to said MBIST engine.

8. A method for detecting degradation in an integrated circuit as recited in claim 1 the step of providing at least one monitor element coupled to said MBIST engine includes the steps of providing at least one monitor element applied to at least one of data arrays and registers; said at least one monitor element used with said MBIST engine to insure correct operation of said at least one of data arrays and registers with a defined degree of margin.

9. A method for detecting degradation in an integrated circuit as recited in claim 8 wherein said at least one monitor element is used with said MBIST engine to identify an approaching failing situation, thereby enabling appropriate preventative action.

10. A method for detecting degradation in an integrated circuit as recited in claim 1 wherein the step of utilizing said MBIST engine for controlling operation of said at least one monitor element and communicating monitor bits includes the steps of generating a predefined data pattern utilizing said MBIST engine.

11. A method for detecting degradation in an integrated circuit as recited in claim 1 wherein said at least one monitor element is defined by at least one monitor bit line of a memory array; and the step of utilizing said MBIST engine for controlling operation of said at least one monitor element and communicating monitor bits includes the steps of writing monitor bits with refresh commands.

12. A method for detecting degradation in an integrated circuit as recited in claim 1 wherein said at least one monitor element is defined by at least one monitor bit line of a memory array; and the step of utilizing said MBIST engine for controlling operation of said at least one monitor element and communicating monitor bits includes the steps of writing monitor bits by accessing each row location with said MBIST engine generating a predefined data pattern.

13. A method for detecting degradation in an integrated circuit as recited in claim 1 wherein said at least one monitor element is defined by at least one monitor word line of a memory array; and the step of utilizing said MBIST engine for controlling operation of said at least one monitor element and communicating monitor bits includes the steps of writing monitor bits with refresh commands with said MBIST engine generating a predefined data pattern.

14. A method for detecting degradation in an integrated circuit as recited in claim 1 wherein the step of utilizing said MBIST engine for controlling operation of said at least one monitor element and communicating monitor bits includes the steps of providing MBIST control circuitry for initializing monitor bits to a known value; utilizing said MBIST control circuitry to control one or more functions including access, restore, address control, data generation, data compare, and refresh functions associated with the monitor bits.

15. A method for detecting degradation in an integrated circuit as recited in claim 1 wherein the step of utilizing said MBIST engine for controlling operation of said at least one monitor element and communicating monitor bits includes the steps of providing latch circuitry for the monitor bits, said latch circuitry used to communicate to and from said MBIST engine.

16. A method for detecting degradation in an integrated circuit as recited in claim 1 wherein said at least one monitor element is defined by a separate array and the step of utilizing said MBIST engine for controlling operation of said at least one monitor element and communicating monitor bits includes the steps of generating one of a fixed predefined data pattern or a dynamically changing data pattern utilizing said MBIST engine.

17. Apparatus for detecting degradation in an integrated circuit and the integrated circuit includes a memory array, said apparatus comprising:

a monitor built-in self-test (MBIST) engine;

at least one monitor element coupled to said MBIST engine; said at least one monitor element including at least one of a monitor bit line of the memory array, a monitor word line of the memory array or a separate array including unique word lines, bit lines, and control and sense circuitry;

said MBIST engine for controlling operation of said at least one monitor element for communicating monitor bits; and for identifying degradation of signal, timing and voltage margins utilizing said at least one monitor element.

18. Apparatus for detecting degradation in an integrated circuit as recited in claim 17 wherein said MBIST engine includes MBIST control circuitry and MBIST registers coupled to said at least one monitor element.

19. Apparatus for detecting degradation in an integrated circuit as recited in claim 17 wherein at least one monitor element includes unused circuit elements or instantiations of said unused circuit elements in the integrated circuit.

20. Apparatus for detecting degradation in an integrated circuit as recited in claim 17 includes latch circuitry for the monitor bits, said latch circuitry used to communicate to and from said MBIST engine.